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Room-Temperature Negative Differential Resistance in Graphene Field Effect Transistors: Experiments and Theory

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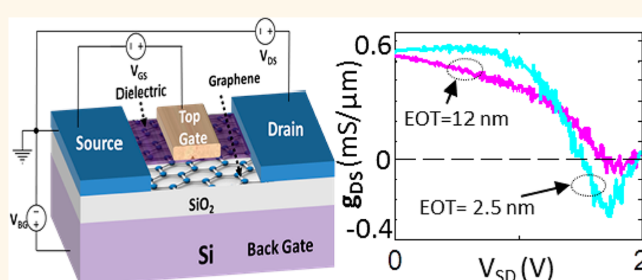
ABSTRACT In this paper we demonstrate experimentally and discuss the negative differential resistance (NDR) in dual-gated graphene field effect transistors (GFETs) at room temperature for various channel lengths, ranging from 200 nm to 5 μm. The GFETs were fabricated using chemically vapor-deposited graphene with a top gate oxide down to 2.5 nm of equivalent oxide thickness (EOT). We originally explain and demonstrate with systematic simulations that the onset of NDR occurs in the unipolar region itself and that the main mechanism behind NDR is associated with the competition between the specific field dependence of carrier density and the drift velocity in GFET. Finally, we show experimentally that NDR behavior can still be obtained with devices of higher EOTs; however, this comes at the cost of requiring higher bias values and achieving lower NDR level.



KEYWORDS: graphene · field effect transistor · negative differential resistance · chemical vapor deposition

Graphene, a two-dimensional material, has generated great interest in electronic devices since its successful demonstration in 2004.[1,2] A number of novel and promising physical characteristics have been found for this material. One such prominent characteristic, which has been the subject of only a few experimental studies,[3−5] is the negative differential resistance (NDR). NDR is a particularly useful property because of its utility in applications such as oscillators,[6] reflection amplifiers,[7] logic switches,[8] and memories.[9] The ability to modulate the concentration of charge carriers *via* the electrostatic gate and the carrier-dependent saturation velocity at high fields are some of the unique properties of graphene. The NDR, as described in this work, stems from these effects. The NDR behavior in graphene using tunneling through p−n junctions or nanoribbons has also been proposed theoretically;[10−13] however, the realization of such devices is extremely difficult due to the complexity involved in their fabrication. NDR was also observed in other technologies and devices such as resonant tunnel diode,[14] single electron transistor,[15] Esaki diode,[16] *etc.* with high peak-to-valley current ratios. Yet these technologies suffer from low peak current density. A graphene field effect transistor (GFET) is a promising candidate for NDR devices because of its high current carrying capabilities.[17]

The mechanism behind NDR in GFET has been discussed in ref 3 in which the explanation was mainly based on the evolution of charge carrier distribution in the channel. The key problem with this explanation, however, is that it does not take into account velocity saturation, which plays an important role in the high field transport of graphene. The drain current flowing in a transistor is the product of charge and velocity. Therefore, to explain any nonlinearity in current characteristics, one must take both these quantities into account. In this work, we originally explain and demonstrate with systematic simulations that the main mechanism behind NDR is associated with the competition between the charge and velocity in the GFET.

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In addition to the proposed novel mechanism, we report a rigorous experimental work with GFET, whose channel lengths range between 200 nm and 5 μm and which conditionally show NDR. Importantly, the top-gated GFET used here have been fabricated using graphene grown by an industry-friendly chemical vapor deposition (CVD) process and transferred on CMOS-compatible silicon substrate. This approach opens up the opportunity for large-scale fabrication of high performance NDR graphene devices. Finally, we experimentally demonstrate the dependence of the NDR level on the oxide thickness. To the best of our knowledge this is the first work that studies this.

RESULTS AND DISCUSSION

In this work, we present NDR behavior under certain biasing conditions in GFETs fabricated using graphene grown by the CVD process (see Methods). The GFETs, which are used in this work, employ a thin layer (~5 nm) of Hafnium dioxide (HfO_2) as a top gate dielectric, unless otherwise stated. A simplified sketch of the fabricated GFET is shown in Figure 1a. Figure 1b shows the scanning electron micrograph (SEM) image of a well aligned device with gate length 500 nm and with 50 nm of ungated region between the gate and the source/drain. Short ungated regions and large widths reduce the series resistance. This is crucial for achieving measurable NDR, as discussed later. We present the room temperature measurement results of a similar device with a width of 30 μm. The use of Si substrate as a back gate allows control over the series resistance of the device and also allows the estimation of the top-gate dielectric capacitance. The estimated top gate capacitance (C_{TG}) and its EOT value are 1.4 μFcm^{-2} and 2.5 nm, respectively (see Supporting Information). Using the model proposed in ref 18, the hole and electron mobilities of the device are found to be 3525 cm^2/(V s) and 3082 cm^2/(V s), respectively (see Supporting Information).

Figure 1c shows the output characteristics of the representative 500 nm gate length device. Under the bias $V_{BG} = -40$ V, $V_{GS} = -1.5$ V and $V_{SD} > 1.5$ V, we see a change in the monotony of drain current, resulting in NDR. Figure 1d shows the corresponding differential conductance g_{DS} = (dI_{SD}/dV_{SD}) confirming the NDR region for $V_{SD} > 1.5$ V. As it can be seen, the NDR is observed at $V_{BG} = -40$ V and not at $V_{BG} = 0$ V. This is mainly due to the lower series resistance at $V_{BG} = -40$ V than at $V_{BG} = 0$ V. The lower series resistance for $V_{BG} = -40$ V as compared to $V_{BG} = 0$ V is evident from the saturating current characteristics at high top gate voltages in the hole branch (see Figure S3a in the Supporting Information). A characteristic signature of NDR is reflected in its transfer characteristics at $V_{BG} = -40$ V shown in Figure 1e. As source-drain voltage V_{SD} increases, the Dirac point shifts in the negative direction, ultimately leading to crossing of transfer curves in the hole branch. From the constant top gate voltage slice ($V_{GS} = -1.5$ V), the drain current is plotted for different V_{SD} in Figure 1f showing the NDR characteristics.

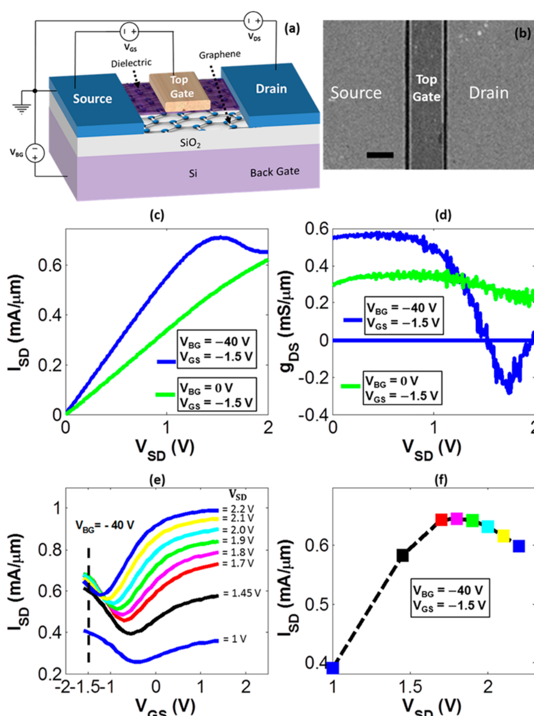

Figure 1. (a) Schematic of a GFET on Si/SiO_2 substrate; (b) top view SEM with 400 nm scale bar; (c) drain current (I_{SD}) as a function of source drain voltage (V_{SD}) of a GFET with gate length L_G = 500 nm and width W = 30 μm at different top gate and back gate biases; (d) corresponding differential conductance (g_{DS}) as a function of V_{SD}; (e) transfer characteristics of the same GFET at different drain biases for back gate bias $V_{BG} = -40$ V; (f) I_{SD} as a function of V_{SD} obtained from the transfer characteristics for $V_{GS} = -1.5$ V.

Next we discuss the biasing conditions for achieving NDR. The GFET needs to be biased at a high $|V_{GS\text{-}EFF}|$, which is defined as $V_{GS\text{-}EFF} = V_{GS} - V_{Dirac\text{-}Top}$ where $V_{Dirac\text{-}Top}$ is the top-gate voltage for which the current is minimum, and then the drain voltage should be swept so that the total carriers in the channel decrease. The local carrier density at a position x in the channel can be approximately expressed as $n(x) = |C_{TG\text{-}tot}\,(V_{GS\text{-}EFF} - V(x))/q|$ where $C_{TG\text{-}tot}$ is the total top-gate oxide capacitance, q is the electronic charge, and $V(x)$ is the potential in the channel which is zero at $x = 0$ and equal to V_{DS} at $x = L$. Therefore, if $V_{GS\text{-}EFF}$ is negative, V_{DS} should be swept negatively so as to decrease $n(x)$. As illustrated in Figure 1c, when the device was biased in negative $V_{GS\text{-}EFF}$, NDR was achieved when drain voltage was negative. However, when $V_{GS\text{-}EFF}$ was positive, NDR was not observed for negative values of V_{DS} (see Figure S4 in the Supporting Information). This is because of the increase in the number of carriers in channel as V_{DS} increases negatively. This increase results in increasing g_{DS} which goes against the NDR phenomenon.

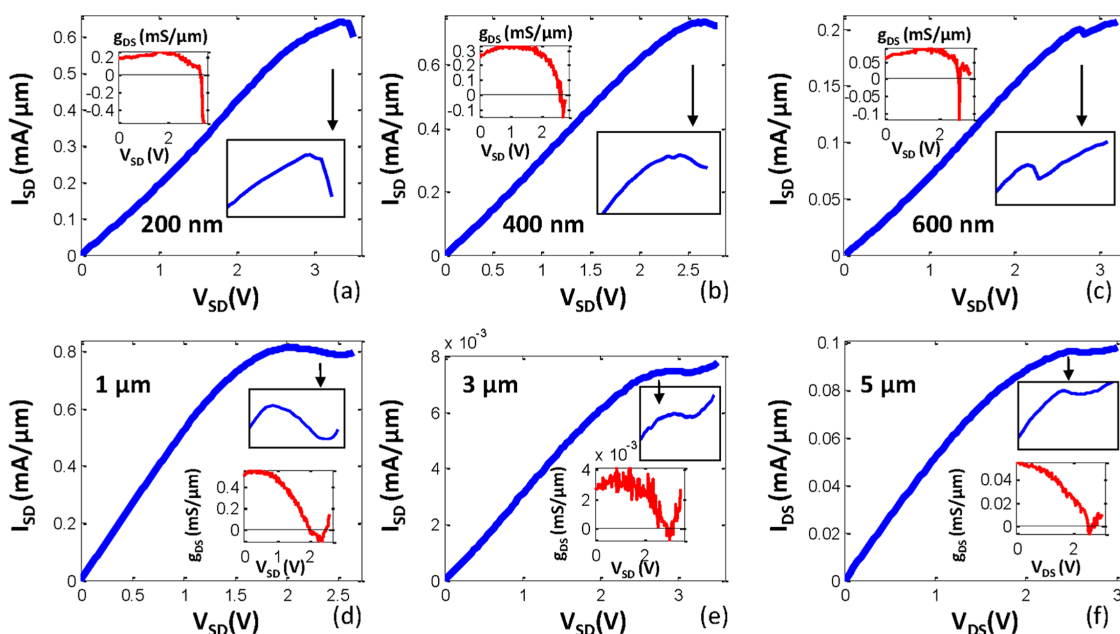

Figure 2. Drain current as a function of drain voltage and the corresponding differential conductance (g_{DS}) as a function of drain voltage in the inset for (a) L_G = 200 nm, W = 19 μm, at V_{GS} = −3.2 V, V_{BG} = −40 V; (b) L_G = 400 nm, W = 40 μm, at V_{GS} = −2.3 V, V_{BG} = −40 V; (c) L_G = 600 nm, W = 40 μm, at V_{GS} = −3.5 V, V_{BG} = −40 V; (d) L_G = 1 μm, W = 20 μm, at V_{GS} = −1.7 V, V_{BG} = −40 V; (e) L_G = 3 μm, W = 19 μm, at V_{GS} = −3.5 V, V_{BG} = −40 V; and (f) L_G = 5 μm, W = 19 μm, at V_{GS} = 2.5 V, V_{BG} = −40 V.

Figure 2 shows the output characteristics of several graphene devices with gate lengths from 200 nm to 5 μm, all exhibiting NDR. The NDR characteristics obtained for these devices were stable after repeating the measurements several times. Most of the devices showed NDR in the hole branch due to the higher hole mobility of the samples. However, Figure 2f shows the NDR obtained, also, for positive $V_{GS\text{-}EFF}$ and positive drain voltage (electron branch) which is yet another possible biasing condition to achieve NDR.

To explain the mechanism behind the NDR phenomenon observed in our experiments, we use a standard drift diffusion model[19] for drain current in the channel which can be expressed as

$$I_{DS} = q\,\frac{W}{L}\int_0^L n(x)\,v_{drift}(x)\,dx \qquad (1)$$

where v_{drift} is the drift velocity. The carrier density, $n(x)$, can be calculated more accurately[20,21] as $n(x) = n_0 + |-(^1/_{2q})C_Q(x)\,\Phi(x)|$ where n_0 is the residual carrier density. C_Q is the quantum capacitance given by $C_Q(x) = (2q^3|\Phi(x)|)/(\pi(\hbar v_f)^2)$, where $\hbar$ is the reduced Planck constant, v_f is the Fermi velocity in graphene, and $\Phi(x)$ is the potential across C_Q given by $\Phi(x) = (C_{TG}/(C_{TG} + C_Q(x)))(V_{GS} - V_{Dirac\text{-}Top} - V(x))$. As the quantities C_Q and Φ depend on each other, they need to be solved self-consistently for the final estimation of $n(x)$. The drift velocity is given as $v_{drift} = (\mu_0|E|)/(1 + ((\mu_0|E|)/v_{sat}))$, where μ_0 is the low field mobility, E is the longitudinal electric field, and v_{sat} is the carrier dependent saturation velocity,[19] with $v_{sat}(x) = \Omega/(\pi n(x))^{1/2}$ where Ω is the phonon energy.

As explained in the model above, the drain current depends on the carrier density and the drift velocity. We believe that NDR phenomena occur due to the competition between these two quantities. As drain voltage increases, the following happens: (1) The total number of carriers in the channel decreases if the GFET is biased appropriately as discussed previously, and (2) the drift velocity increases owing to the electric field increase. Effect 1 favors the NDR phenomenon, whereas effect 2 opposes it. At high drain voltages, however, v_{drift} saturates to v_{sat} which may further favor the NDR phenomena to occur. This effect is explained in the simulated characteristics below. Figure 3a shows the simulated output characteristics for a 500 nm long device with parameters: EOT = 2.5 nm, Ω = 60 meV, μ_0 = 2000 cm^2/(V s), $n_0 = 2.2 \times 10^{11}$ cm^{-2} and $V_{Dirac\text{-}Top}$ = 0 V. The green curve with V_{GS} = −0.5 V, shows only positive values of g_{DS}, whereas the red curve with V_{GS} = −1 V exhibits NDR starting from V_{SD} = 0.86 V until V_{SD} = 1.12 V. We now focus on the contribution of effect 1 on the curves with NDR (red) and without NDR (green). A good indicator of total number of carriers in the channel is the average carrier density, defined as $\langle n\rangle = {}^1/_L\int_0^L n(x)dx$ and shown in Figure 3b. As expected, the total carriers in the channel decreases initially with the drain voltage. For instance, the decrease in carriers for the red curve happens until V_{SD} = 1.45 V and then it increases again. It is interesting to note that the rate of decrease of carriers is the same for both red and green curves; however, the NDR was only seen for red curve. Therefore, it is also important to consider effect 2 which is about v_{drift}. As shown in Figure 3c, v_{drift} initially

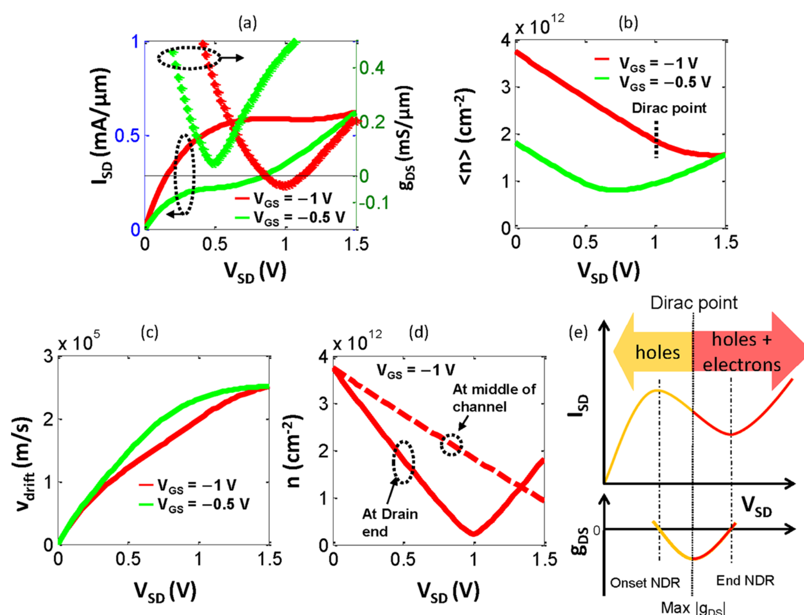

Figure 3. (a) Simulated drain current I_{SD} (solid line) as a function of source drain voltage V_{SD} for $V_{GS} = -1$ V (red) and $V_{GS} = -0.5$ V (green) and corresponding g_{DS} (dotted line) as a function of V_{SD}. The gate length L_G is 500 nm and EOT is = 2.5 nm; (b) simulated average carrier density in the channel, $\langle n \rangle$, as a function of V_{SD} for $V_{GS} = -1$ V (red) and $V_{GS} = -0.5$ V (green); (c) simulated drift velocity as a function of V_{SD}; (d) simulated carrier density, n, at drain end (solid line) and at the middle of channel (dotted line) as a function of V_{SD} for $V_{GS} = -1$ V; (e) simplified sketch of the mechanism of NDR. The orange shaded portion corresponds to the hole-dominated channel and the red shaded portion corresponds to the region when both electron and holes are present in the channel.

increases due to electric field increase but then saturates to v_{sat}. Interestingly, we see that v_{drift} for the red curve is smaller than that of the green curve mainly around the range where NDR is observed. This can be explained by the carrier density dependent v_{sat} ($\propto 1/n$). At high $V_{GS} = -1$ V, there are more carriers in the channel than at $V_{GS} = -0.5$ V which means lower v_{sat} ($\propto 1/n$) and hence lower v_{drift} value for $V_{GS} = -1$ V. This is the main reason for the NDR to occur, that is, reduced drift velocity due to carrier density-dependent v_{sat} or, in other words, the lowering of the effective carrier mobility.

Further, it is interesting to note that the onset of NDR takes place in the unipolar region and before the Dirac point enters the channel. The Dirac point enters the channel when the drain voltage $V_{SD} = 1$ V (Figure 3d), whereas the NDR starts at $V_{SD} = 0.86$ V (Figure 3a). This is the another key indication that reduced v_{drift} is indeed the cause of NDR and not the change of carrier types.[3] In fact, it is observed that when the Dirac point enters the channel, the magnitude of NDR reaches its maximum (maximum negative g_{DS} point at $V_{SD} = 1$ V as shown in Figure 3a). This can be explained by focusing on the red curve in Figure 3b. After V_{SD} = 1 V, electrons enter the channel (Dirac point highlighted in Figure 3b). However, the decrease in the total number of carriers continues beyond $V_{SD} = 1$ V. This decrease in total carriers in the channel is solely attributed to electrons (minority carriers in channel) replacing holes (majority carriers in channel) with lower carrier density. Interestingly, this decrease is slower than the decrease observed below $V_{SD} = 1$ V (from 0 to 1 V) as can be seen clearly in Figure 3b. This slower decrease is the cause of decrease in magnitude of negative g_{DS} after the Dirac point enters the channel. In addition, the NDR region continues until $V_{SD} = 1.12$ V and not until the Dirac point reaches the middle of the channel[3] which happens at much higher $V_{SD} > 1.5$ V (Figure 3d). In summary, the relation between the position of the Dirac point entering the channel and the NDR region is illustrated in Figure 3e.

Finally we demonstrate the dependence of the NDR phenomena on the dielectric thickness. Han *et al.*[5] rightly pointed out that as EOT scales down, the drop of carrier density *versus* drain voltage increases; that is, the fast drop in carrier density helps the saturation phenomena to occur. This can also be correlated to the NDR phenomena. Figure 4a shows the simulated average carrier density $\langle n \rangle$ normalized to its value at $V_{SD} = 0$ V as a function of V_{SD} for different thicknesses of EOT. Clearly, as EOT increases, the rate of drop in the carrier density *versus* V_{SD} decreases and this does not favor the NDR phenomena. However, NDR may still be observed for higher EOTs with the help of reducing the v_{drift} (effect 2), that is, either by applying a high gate voltage or if the samples have a lower v_{sat} value. As it can be seen in Figure 4b, NDR was experimentally observed for a device with larger EOT ≈ 12 nm (15 nm Al_2O_3) and with lateral dimensions the same as our central geometry (L_G = 500 nm, $W = 30$ μm). A comparison of results of the

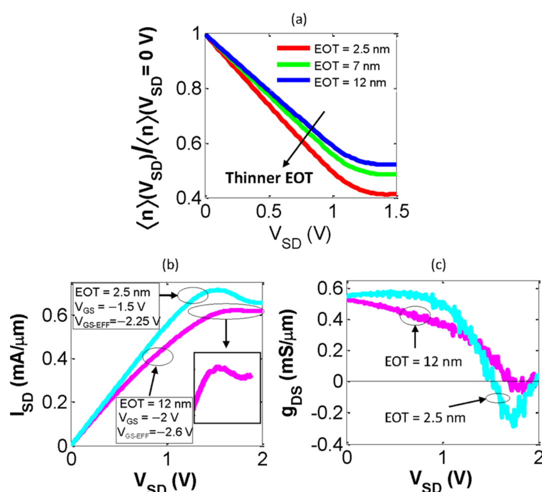

Figure 4. (a) Simulated average carrier density $\langle n \rangle$ normalized to it value at V_{SD} = 0 V as a function of V_{SD} for 500 nm GFET with EOT 2.5, 7, and 12 nm at $V_{GS} = -1$ V. (b) Measured I_{SD} *versus* V_{SD} for two EOTs with gate length L_G = 500 nm and W = 30 μm at bias voltages $V_{BG} = -40$ V. The $V_{Dirac\text{-}Top}$ (at $V_{BG} = -40$ V) values for EOT = 2.5 nm and EOT = 12 nm were 0.75 and 0.6 V, respectively. (c) Corresponding measured g_{DS} *versus* V_{SD} characteristics.

two EOTs reveals two expected points. First, the NDR for EOT = 12 nm occurs at higher gate voltage as compared with the NDR for EOT = 2.5 nm as shown in Figure 4b. Second, the magnitude of maximum negative g_{DS} is lower for the higher EOT, as can be seen in Figure 4c, which is also in accordance with the higher relative decrease of the average carrier density of the channel for the smaller EOTs as shown in Figure 4a.

CONCLUSIONS

Top-gated GFET of various gate lengths and dielectric thicknesses were fabricated and the observation of NDR was reported under certain biasing conditions. The mechanism behind NDR was also explained in detail using the standard drift diffusion model. The main conclusion is that NDR behavior happens due to the competition between two core quantities of the GFET: the total number of carriers in the channel and their drift velocity. Further, it was analyzed with simulations and demonstrated experimentally that lower EOTs provide a higher NDR level. The successful demonstration of NDR using large area graphene grown from CVD opens up an alternative route in the field of graphene research particularly for its utilization in key applications such as oscillators, amplifiers, memories, and fast switches.

METHODS

CVD Graphene Growth and Transfer. The graphene samples used in this work were grown on Cu film *via* a CVD process.[22] The growth was carried out in a horizontal tubular furnace. A Cu foil (99.98% from Sigma-Aldrich) was annealed at 1000 °C for 30 min in 3 Torr of H_2 with the chamber being closed by a valve. Then a pulse of CH_4 was introduced. The growth occurs for 3 min, at 1000 °C under 19 Torr. After the growth, the graphene was transferred onto a Si/SiO_2 substrate using a typical CVD transfer process.[23] To transfer the graphene, we first spin coated (4000 rpm, 1 min) a layer of poly(methyl methacrylate) (PMMA) on graphene/Cu sample. The Cu was then etched away by floating the PMMA/graphene/Cu sample on 1 M ammonium persulfate. The PMMA/graphene film was washed with 1 M HCl and DI water for several times. Finally, the PMMA/graphene was transferred to the Si substrate with 295 nm thick thermal oxide. The PMMA coating was removed with acetone and the substrate was rinsed with isopropyl alcohol. The quality of graphene before and after the transfer was characterized using Raman spectroscopy, suggesting continuous single layer graphene with few defects (see Supporting Information).

GFET Fabrication. Device active regions were patterned using electron beam lithography and subsequent oxygen plasma etching. The source and drain electrodes made of Ti/Pd/Au (1 nm/20 nm/40 nm thick) were fabricated by second electron beam lithography and liftoff. To form the top gate oxide, a seed layer[18] of Al (~1.5 nm) was thermally oxidized (120 °C, 6 h) on graphene before atomic layer deposition of either a 5 nm-thick HfO_2 or a 15 nm-thick Al_2O_3 layer. Finally, the metal stack Ti/Au (20 nm/40 nm) was deposited as the top-gate electrode. Measurements were carried out at room temperature using a HP 4145B semiconductor parameter analyzer.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Detailed characterization of graphene quality, oxide capacitance, EOT, and mobility calculations, and other measured characteristics. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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